REMARKS

This application has been reviewed in light of the Office Action dated June 14, 2007. Claims 1-7 are now pending in the application. Claims 1, 5, 6 and 7 have been amended. No new matter has been added. The Examiner's reconsideration of the rejection in view of the following remarks is respectfully requested.

By the Office Action, the Examiner requested the submission of the references cited in the application. A separate **Information Disclosure Statement** will be submitted.

By the office action, claims 6 and 7 were objected to as being directed to multiple dependent claims dependent from claim 5 which was also a multiple dependent claim. Claims 5, 6 and 7 have been amended in a way believed to overcome the objection. Reconsideration of the rejection is earnestly solicited.

By the Office Action, claims 1-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,667,783 to Greene et al. (herein after Greene) in view of U.S. Patent No. 5,748,169 to Okumura et al. (hereinafter Okumura).

Claim 1 recites, *inter alia*, an active matrix liquid crystal display device having ... sets of selection and data address conductors connected to the picture elements, and a set of connection lines for supplying selection signals to the set of selection address conductors, ... wherein each picture element includes a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row, and wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of

picture elements.

Greene teaches a pixel array with column and row address lines (200 and 202) terminating on the same sides of the array. As the Examiner admits, Greene does not disclose or suggest that each picture element includes a storage capacitor connected between the picture element electrode and a capacitor line shared by the picture elements in the same row, and wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of picture elements. Further, Greene does not disclosure or suggest a solution to the issues raised and solved in the present application.

The Examiner cites Okumura to cure these deficiencies. In FIG. 14 of Okumura, a structure is shown where the gate lines 21 connect to a gate of a transistor device 25 and to a capacitor 26 of a next adjacent row. Okumura does not disclose or suggest at least a capacitor line as set forth in the present claim 1. For example, Okumura fails to disclose or suggest at least "wherein the selection address conductor associated with one row of picture elements is coupled to the capacitor line associated with a different row of picture elements so that each connection line is connected to a respective selection address conductor for one row of picture elements and its coupled capacitor line for another row of picture elements".

Greene and/or Okumura taken singly or in combination do not teach or suggest a capacitor line as a completely separate element that is in addition to a selection address conductor (and a data address conductor). Greene teaches connections to address lines but does not disclose or suggest a separate capacitor line that is disposed within a pixel array where the capacitor line is associated with a row of picture elements. Likewise, Okumura provides a gate line that connects directly to

capacitors in a next row, but there is no teaching or suggestion of a separate capacitor line as recited in the present claims.

Claim 1 of the present invention includes selection address lines, data address lines, connection lines and a capacitor line. Further, the capacitor line is included to reduce or eliminate parasitic capacitive effects suffered by other display devices as stated in the present specification with reference to FIGS. 1 and 2 (see also the specification at page 9). No motivation is provided in either Okumura or Greene to provide a capacitor line as recited in present claim 1. Note that, in FIG. 14 of Okumura, the connection between the capacitors 26 and the next adjacent row's gate line 21 passes directly through the pixel cell itself. As such, the structure shown in FIG. 14 would suffer from the parasitic capacitance issues addressed in the present specification with reference to FIGS. 1 and 2. Namely, a parasitic capacitance would form in parallel with the gate capacitance of the switching transistor resulting in errors in the display brightness levels. (See specification at page 9). Both Greene and Okumura are silent on this problem, and one skilled in the art with knowledge of the cited references would not arrive at the structure of present invention as set forth in claim 1.

Therefore, even if the cited references are combined there is no teaching or suggestion for a separate capacitor line to solve parasitic capacitance issues. Since the cited combination fails to teach or suggest all of the elements of claim 1, claim 1 is believed to be in condition for allowance over the cited combination. Reconsideration of the rejection is respectfully requested for at least the stated reasons.

Claims 2-7 are also believed to be in condition for allowance due at least to their dependency from claim 1. Other reasons exist for allowing these claim as well. For example, claim 3 recites that a selection address conductor and a capacitor line are coupled by an interconnection between their ends at one side of the array. The cited combination does not teach a capacitor line, and therefore

cannot teach that the capacitor line is coupled by an interconnection to a selection address conductor.

In another example, claim 6 recites that the capacitor line and selection address conductor associated with one row of picture elements extend along opposite sides of the row of picture elements. The cited combination does not teach a capacitor line, and therefore cannot teach that the capacitor line extends on an opposite side of a pixel row from a selection address conductor.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's representatives Deposit Account No. 14-1270.

Respectfully submitted,

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